

240pin Unbuffered DDR3 SDRAM MODULE

Based on 128Mx8 DDR3 SDRAM C Die

Features

• Performance:

Speed Sort		PC3-8500	PC3-10600	Unit
		-BE	-CG	
DIMM $\overline{\text{CAS}}$ Latency		7	9	
f_{CK}	Clock Frequency	533	667	MHz
t_{CK}	Clock Cycle	1.875	1.5	ns
f_{DQ}	DQ Burst Frequency	1066	1333	Mbps

- JEDEC Standard 240-pin Dual In-Line Memory Module
- 256Mx64 DDR3 Unbuffered DIMM based on 128Mx8 DDR3 Elixir SDRAM
- Intended for 533MHz and 667MHz applications
- Inputs and outputs are SSTL15 compatible
- $V_{\text{DD}} = V_{\text{DDQ}} = 1.5\text{V} \pm 0.075\text{V}$
- SDRAMs have 8 internal banks for concurrent operation
- Differential clock inputs
- Data is read or written on both clock edges
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Extended operating temperature range
- Auto Self-Refresh option
- Automatic and controlled precharge commands
- Programmable Operation:
 - DIMM $\overline{\text{CAS}}$ Latency: 6,7,8,9,
 - Burst Type: Sequential & Interleave
 - Burst Length: BC4, BL8
 - Operation: Burst Read and Write
- 14/10/2 Addressing (row/column/rank) – 2GB
- Serial Presence Detect
- Gold contacts
- SDRAMs in 78 BGA Package
- RoHS compliance

Description

M2Y2G64CB8HC5N and M2Y2G64CB8HC9N are 240-Pin Double Data Rate 3 (DDR3) Synchronous DRAM Unbuffered Dual In-Line Memory Module (UDIMM), two ranks 256Mx64 high-speed memory array. M2Y2G64CB8HC5N and M2Y2G64CB8HC9N use sixteen 128Mx8 DDR3 SDRAMs. These DIMMs are manufactured using raw cards developed for broad industry use as reference designs. The use of these common design files minimizes electrical variation between suppliers. All Elixir DDR3 SDRAM DIMMs provide a high-performance, flexible 8-byte interface in a 5.25" long space-saving footprint.

The DIMM is intended for use in applications operating up to 533 MHz or 667MHz clock speeds and achieves high-speed data transfer rates of up to 1066Mbps or 1333 Mbps. Prior to any access operation, the device $\overline{\text{CAS}}$ latency and burst / length / operation type must be programmed into the DIMM by address inputs A0-A13 and I/O inputs BA0, BA1, and BA2 are using for the mode register set cycle.

The DIMM uses serial presence-detect implemented via a serial 2,048-bit EEPROM using a standard IIC protocol. The first 128 bytes of serial PD data are programmed and locked during module assembly. The remaining 128 bytes are available for use by the customer.

Ordering Information

Part Number	Speed			Organization	Leads	Power	Note
M2Y2G64CB8HC5N-BE	533MHz (1.875ns@ CL = 7)	DDR3-1066	PC3-8500	256Mx64	Gold	1.5V	
M2Y2G64CB8HC5N-CG	667MHz (1.500ns@ CL = 9)	DDR3-1333	PC3-10600				
M2Y2G64CB8HC9N-BE	533MHz (1.875ns@ CL = 7)	DDR3-1066	PC3-8500				
M2Y2G64CB8HC9N-CG	667MHz (1.500ns@ CL = 9)	DDR3-1333	PC3-10600				

Pin Description

Pin Name	Description	Pin Name	Description
CK0, CK1	Clock Inputs, positive line	DQ0-DQ63	Data input/output
$\overline{\text{CK0}}, \overline{\text{CK1}}$	Clock Inputs, negative line	DQS0-DQS8	Data strobes
CKE0, CKE1	Clock Enable	$\overline{\text{DQS0}}, \overline{\text{DQS8}}$	Data strobes complement
$\overline{\text{RAS}}$	Row Address Strobe	DM0-DM8	Data Masks
$\overline{\text{CAS}}$	Column Address Strobe	$\overline{\text{EVENT}}$	Temperature event pin
$\overline{\text{WE}}$	Write Enable	$\overline{\text{RESET}}$	Reset pin
$\overline{\text{S0}}, \overline{\text{S1}}$	Chip Selects	$\text{V}_{\text{REFDQ}}, \text{V}_{\text{REFCA}}$	Input/Output Reference
A0-A9, A11, A13	Address Inputs	V_{DDSPD}	SPD and Temp sensor power
A10/AP	Address Input/Auto-Precharge	SA0, SA1	Serial Presence Detect Address Inputs
A12/ $\overline{\text{BC}}$	Address Input/Burst Chop	Vtt	Termination voltage
BA0-BA2	SDRAM Bank Address Inputs	Vss	Ground
ODT0, ODT1	Active termination control lines	VDD	Core and I/O power
SCL	Serial Presence Detect Clock Input	NC	No Connect
SDA	Serial Presence Detect Data input/output		

Pinout

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{REFDQ}	121	V _{SS}	31	DQ25	151	V _{SS}	61	A2	181	A1	91	DQ41	211	V _{SS}
2	V _{SS}	122	DQ4	32	V _{SS}	152	DM3	62	V _{DD}	182	V _{DD}	92	V _{SS}	212	DM5
3	DQ0	123	DQ5	33	$\overline{\text{DQS3}}$	153	NC	63	CK1/NC	183	V _{DD}	93	$\overline{\text{DQS5}}$	213	NC
4	DQ1	124	V _{SS}	34	DQS3	154	V _{SS}	64	$\overline{\text{CK1}}/\text{NC}$	184	CK0	94	DQS5	214	V _{SS}
5	V _{SS}	125	DM0	35	V _{SS}	155	DQ30	65	V _{DD}	185	$\overline{\text{CK0}}$	95	V _{SS}	215	DQ46
6	$\overline{\text{DQS0}}$	126	NC	36	DQ26	156	DQ31	66	V _{DD}	186	V _{DD}	96	DQ42	216	DQ47
7	DQS0	127	V _{SS}	37	DQ27	157	V _{SS}	67	V _{REFCA}	187	$\overline{\text{EVENT}}$	97	DQ43	217	V _{SS}
8	V _{SS}	128	DQ6	38	V _{SS}	158	NC	68	NC	188	A0	98	V _{SS}	218	DQ52
9	DQ2	129	DQ7	39	NC	159	NC	69	V _{DD}	189	V _{DD}	99	DQ48	219	DQ53
10	DQ3	130	V _{SS}	40	NC	160	V _{SS}	70	A10/AP	190	BA1	100	DQ49	220	V _{SS}
11	V _{SS}	131	DQ12	41	V _{SS}	161	DM8	71	BA0	191	V _{DD}	101	V _{SS}	221	DM6
12	DQ8	132	DQ13	42	$\overline{\text{DQS8}}$	162	NC	72	V _{DD}	192	$\overline{\text{RAS}}$	102	$\overline{\text{DQS6}}$	222	NC
13	DQ9	133	V _{SS}	43	DQS8	163	V _{SS}	73	$\overline{\text{WE}}$	193	$\overline{\text{S0}}$	103	DQS6	223	V _{SS}
14	V _{SS}	134	DM1	44	V _{SS}	164	NC	74	$\overline{\text{CAS}}$	194	V _{DD}	104	V _{SS}	224	DQ54
15	$\overline{\text{DQS1}}$	135	NC	45	NC	165	NC	75	V _{DD}	195	ODT0	105	DQ50	225	DQ55
16	DQS1	136	V _{SS}	46	NC	166	V _{SS}	76	$\overline{\text{S1}}/\text{NC}$	196	A13	106	DQ51	226	V _{SS}
17	V _{SS}	137	DQ14	47	V _{SS}	167	NC	77	ODT1/NC	197	V _{DD}	107	V _{SS}	227	DQ60
18	DQ10	138	DQ15	48	NC	168	$\overline{\text{RESET}}$	78	V _{DD}	198	NC	108	DQ56	228	DQ61
19	DQ11	139	V _{SS}	49	NC	169	CKE1/NC	79	NC	199	V _{SS}	109	DQ57	229	V _{SS}
20	V _{SS}	140	DQ20	50	CKE0	170	V _{DD}	80	V _{SS}	200	DQ36	110	V _{SS}	230	DM7
21	DQ16	141	DQ21	51	V _{DD}	171	NC	81	DQ32	201	DQ37	111	$\overline{\text{DQS7}}$	231	NC
22	DQ17	142	V _{SS}	52	BA2	172	NC	82	DQ33	202	V _{SS}	112	DQS7	232	V _{SS}
23	V _{SS}	143	DM2	53	NC	173	V _{DD}	83	V _{SS}	203	DM4	113	V _{SS}	233	DQ62
24	$\overline{\text{DQS2}}$	144	NC	54	V _{DD}	174	A12/ $\overline{\text{BC}}$	84	$\overline{\text{DQS4}}$	204	NC	114	DQ58	234	DQ63
25	DQS2	145	V _{SS}	55	A11	175	A9	85	DQS4	205	V _{SS}	115	DQ59	235	V _{SS}
26	V _{SS}	146	DQ22	56	A7	176	V _{DD}	86	V _{SS}	206	DQ38	116	V _{SS}	236	V _{DDSPD}
27	DQ18	147	DQ23	57	V _{DD}	177	A8	87	DQ34	207	DQ39	117	SA0	237	SA1
28	DQ19	148	V _{SS}	58	A5	178	A6	88	DQ35	208	V _{SS}	118	SCL	238	SDA
29	V _{SS}	149	DQ28	59	A4	179	V _{DD}	89	V _{SS}	209	DQ44	119	SA2	239	V _{SS}
30	DQ24	150	DQ29	60	V _{DD}	180	A3	90	DQ40	210	DQ45	120	V _{TT}	240	V _{TT}

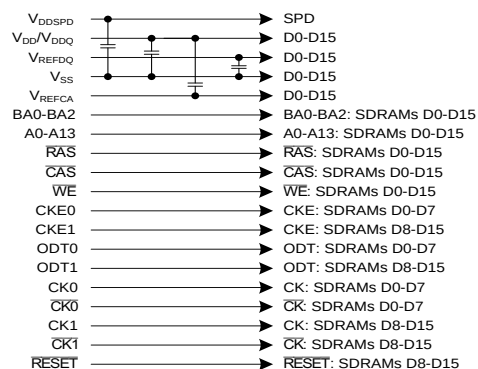
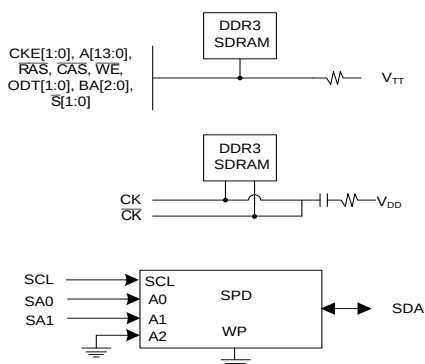
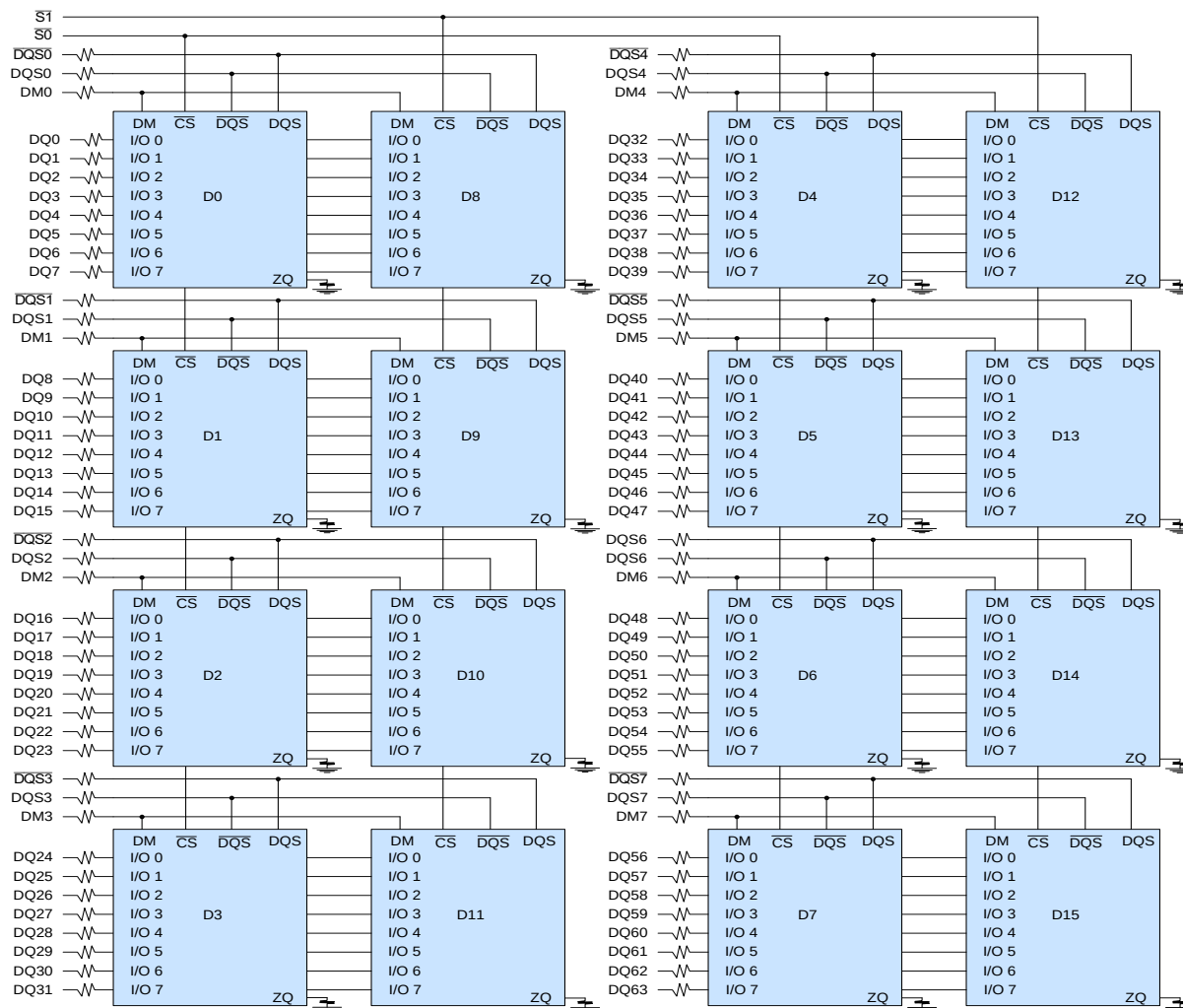
Note: CK1, $\overline{\text{CK1}}$, CKE1, $\overline{\text{S1}}$ and ODT1 are for 2GB modules only.

Input/Output Functional Description

Symbol	Type	Polarity	Function
CK0, CK1 $\overline{\text{CK0}}, \overline{\text{CK1}}$	Input	Cross point	The system clock inputs. All address and command lines are sampled on the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. A Delay Locked Loop (DLL) circuit is driven from the clock inputs and output timing for read operations is synchronized to the input clock.
CKE0, CKE1	Input	Active High	Activates the DDR3 SDRAM CK signal when high and deactivates the CK signal when low. By deactivating the clocks, CKE low initiates the Power Down mode or the Self Refresh mode.
$\overline{\text{S0}}, \overline{\text{S1}}$	Input	Active Low	Enables the associated DDR3 SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue, Rank 0 is selected by $\overline{\text{S0}}$; Rank 1 is selected by $\overline{\text{S1}}$.
$\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$	Input	Active Low	When sampled at the positive rising edge of CK and falling edge of $\overline{\text{CK}}$, signals $\overline{\text{RAS}}, \overline{\text{CAS}}, \overline{\text{WE}}$ define the operation to be executed by the SDRAM.
ODT0, ODT1	Input	Active High	Asserts on-die termination for DQ, DM, DQS, and $\overline{\text{DQS}}$ signals if enabled via the DDR3 SDRAM mode register.
DM0 – DM8	Input	Active High	The data write masks, associated with one data byte. In Write mode, DM operates as a byte mask by allowing input data to be written if it is low but blocks the write operation if it is high. In Read mode, DM lines have no effect.
DQS0 – DQS8 $\overline{\text{DQS0}} – \overline{\text{DQS8}}$	I/O	Cross point	The data strobes, associated with one data byte, sourced with data transfers. In Write mode, the data strobe is sourced by the controller and is centered in the data window. In Read mode, the data strobe is sourced by the DDR3 SDRAM and is sent at the leading edge of the data window. DQS signals are complements, and timing is relative to the cross point of respective DQS and $\overline{\text{DQS}}$. If the module is to be operated in single ended strobe mode, all $\overline{\text{DQS}}$ signals must be tied on the system board to V_{SS} and DDR3 SDRAM mode registers programmed appropriately.
BA0, BA1, BA2	Input	-	Selects which DDR3 SDRAM internal bank of four or eight is activated.
A0 – A9 A10/AP A11 A12/ $\overline{\text{BC}}$ A13	Input	-	During a Bank Activate command cycle, defines the row address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. During a Read or Write command cycle, defines the column address when sampled at the cross point of the rising edge of CK and falling edge of $\overline{\text{CK}}$. In addition to the column address, AP is used to invoke autoprecharge operation at the end of the burst read or write cycle. If AP is high, autoprecharge is selected and BA0-BAn defines the bank to be precharged. If AP is low, autoprecharge is disabled. During a Precharge command cycle, AP is used in conjunction with BA0-BAn to control which bank(s) to precharge. If AP is high, all banks will be precharged regardless of the state of BA0-BAn inputs. If AP is low, then BA0-BAn are used to define which bank to precharge.
DQ0 – DQ63	Input	-	Data Input/Output pins.
$V_{DD}, V_{DDSPD}, V_{SS}$	Supply	-	Power supplies for core, I/O, Serial Presence Detect, Temp sensor, and ground for the module.
V_{REFDQ}, V_{REFCA}	Supply	-	Reference voltage for SSTL15 inputs
SDA	I/O	-	This is a bidirectional pin used to transfer data into or out of the SPD EEPROM and temp sensor. A resistor must be connected from the SDA bus line to V_{DDSPD} on the system planar to act as a pull up.
SCL	Input	-	This signal is used to clock data into and out of the SPD EEPROM and Temp sensor.
SA0 – SA2	Input	-	Address pins used to select the Serial Presence Detect and Temp sensor base address.
$\overline{\text{EVENT}}$	Output	-	The $\overline{\text{EVENT}}$ pin is reserved for use to flag critical module temperature.
$\overline{\text{RESET}}$	Input	-	This signal resets the DDR3 SDRAM

Functional Block Diagram

(2GB, 2 Rank, 128Mx8 DDR3 SDRAMs)



Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. DQ/DQS/DQS/ODT/DM/CKE/S relationships must be maintained as shown.
3. For each DRAM, a unique ZQ resistor is connected to ground. The ZQ resistor is 240Ω ±1%.
4. One SPD exists per module.

Serial Presence Detect -- Part 1 of 2 (2GB)

256Mx64 2 Ranks UNBUFFERED DDR3 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.5V DDR3 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		-BE	-CG	-BE	-CG	
0	CRC range, EEPROM bytes, bytes used	CRC Covers Bytes: 0~116, Total SPD Bytes: 256, SPD Bytes Used: 176,		92		
1	SPD revision	Revision 1.0		10		
2	DRAM device type	DDR3 SDRAM		0B		
3	Module type (form factor)	UDIMM		02		
4	SDRAM Device density and banks	8 banks, 1Gb		02		
5	SDRAM device row and column count	14 rows, 10 columns		11		
6	Module minimum nominal voltage	1.5V		00		
7	Module ranks and device DQ count	2 ranks, 8 bits		09		
8	ECC tag and module memory Bus width	Non ECC, 64bits		03		
9	Fine timebase dividend/divisor (in ps)	2.5ps		52		
10	Medium timebase dividend	1ns		01		
11	Medium timebase divisor	8ns		08		
12	Minimum SDRAM cycle time (tCKmin)(ns)	1.875ns	1.5ns	0F	0C	
13	Reserved	Undefined		00		
14	CAS latencies supported	6,7,8	6,7,8,9	1C	3C	
15	CAS latencies supported	Undefined		00		
16	Minimum CAS latency time (tAmin)(ns)	13.125ns		69		
17	Minimum write recovery time (tWRmin)	15ns		78		
18	Minimum CAS-to-CAS delay (tRCDmin)(ns)	13.125ns		69		
19	Minimum Row Active to Row Active delay (tRRDmin)(ns)	7.5ns	6ns	3C	30	
20	Minimum row Precharge delay (tRPmin)(ns)	13.125ns		69		
21	Upper nibble for tRAS and tRC	1,1		11		
22	Minimum Active-to-Precharge delay (tRASmin)(ns)	37.5ns	36ns	2C	20	
23	Minimum Active-to-Active/Refresh delay (tRCmin)(ns)	50.625ns	49.125ns	95	89	
24	Minimum refresh recovery delay (tRFCmin) LSB	(Combo bytes 24,25)		70		
25	Minimum refresh recovery delay (tRFCmin) MSB	110ns		03		
26	Minimum internal Write-to-Read command delay (tWTRmin)	7.5ns		3C		
27	Minimum internal Read-to-Precharge command delay (tRTPmin)	7.5ns		3C		
28	Minimum four active window delay (tFAWmin) LSB	(Combo byte 28, 29)		01	00	
29	Minimum four active window delay (tFAWmin) MSB	37.5ns	30ns	2C	F0	
30	SDRAM device output drivers supported	RZQ / 7, DLL-Off Mode Support,		82		
31	SDRAM device thermal and refresh options	Extended Temperature Range, ASR,		05		
32	Module thermal sensor	Non Thermal Sensor Support		00		
33	SDRAM device type	Standard Monolithic Device		00		
34-59	Reserved	Undefined		--		
60	Module height (nominal)	29 < height ≤ 30 mm		0F		

M2Y2G64CB8HC5N / M2Y2G64CB8HC9N**2GB: 256M x 64****Unbuffered DDR3 SDRAM DIMM****Serial Presence Detect -- Part 2 of 2 (2GB)**

256Mx64 2 Ranks UNBUFFERED DDR3 SDRAM DIMM based on 128Mx8, 8Banks, 8K Refresh, 1.5V DDR3 SDRAMs with SPD

Byte	Description	SPD Entry Value		Serial PD Data Entry (Hexadecimal)		Note
		-BE	-CG	-BE	-CG	
61	Module thickness (Max)	Back: 1 < thickness ≤ 2 mm, Front: 1 < thickness ≤ 2 mm,		11		
62	Raw Card ID reference	Raw Card B		01		
63	DRAM address mapping edge connector	Undefined		01		
64-116	Reserved	Undefined		--		
117-118	Module manufacture ID	Nanya Technology		830B		
119-125	Module information	Undefined		--		
126-127	CRC	Undefined		4408	06A1	
128-145	Module part number	ASCII values		--		
146	Module die revision	Undefined		00		
147	Module PCB revision	Undefined		00		
148-149	DRAM device manufacturer ID	Nanya Technology		830B		
150-175	Manufacturer reserved	Undefined		--		
176-255	Customer reserved	Undefined		--		

Environmental Requirements

Symbol	Parameter	Rating	Units	Note
T _{OPR}	Module Operating Temperature Range (ambient)	0 to 55	°C	3
H _{OPR}	Operating Humidity (relative)	10 to 90	%	1
T _{STG}	Storage Temperature (Plastic)	-55 to 100	°C	1
H _{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P _{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1, 2

Note:

- Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Up to 9850 ft.
- The component maximum case temperature shall not exceed the value specified in the component spec.

Absolute Maximum DC Ratings

Symbol	Parameter	Rating	Units	Note
V _{DD}	Voltage on VDD pins relative to Vss	-0.4 V ~ 1.975 V	V	1, 3
V _{DDQ}	Voltage on VDDQ pins relative to Vss	-0.4 V ~ 1.975 V	V	1, 3
V _{IN} , V _{OUT}	Voltage on I/O pins relative to Vss	-0.4 V ~ 1.975 V	V	1
T _{STG}	Storage Temperature	-55 to +100	°C	1, 2

Note:

- Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
- VDD and VDDQ must be within 300 mV of each other at all times; and VREF must be not greater

Operating temperature Conditions

Symbol	Parameter	Rating	Units	Note
T _{OPER}	Normal Operating Temperature Range	0 to 85	°C	1, 2
	Extended Temperature Range	85 to 95	°C	1, 3

Note:

- Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JEDEC51-2.
- The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.
- Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:
 - Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8 μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
 - If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 = 0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ	Max	Units	Notes
V _{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V _{DDQ}	Output Supply Voltage	1.425	1.5	1.575	V	1,2

Note:

- Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
- V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.

Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Units	Note
		Min.	Max.	Min.	Max.		
V _{IH.CA} (DC)	DC Input Logic High	V _{ref} + 0.100	V _{DD}	V _{ref} + 0.100	V _{DD}	V	1
V _{IL.CA} (DC)	DC Input Logic Low	V _{SS}	V _{ref} - 0.100	V _{SS}	V _{ref} - 0.100	V	1
V _{IH.CA} (AC)	AC Input Logic High	V _{ref} + 0.175	Note 2	V _{ref} + 0.175	Note 2	V	1, 2
V _{IL.CA} (AC)	AC Input Logic Low	Note 2	V _{ref} - 0.175	Note 2	V _{ref} - 0.175	V	1, 2
V _{IH.CA} (AC150)	AC Input Logic High	-	-	V _{ref} + 0.15	Note 2	V	1, 2
V _{IL.CA} (AC150)	AC Input Logic Low	-	-	Note 2	V _{ref} - 0.15	V	1, 2
V _{RefCA} (DC)	Reference Voltage for ADD, CMD Inputs	0.49 x V _{DD}	0.51 x V _{DD}	0.49 x V _{DD}	0.51 x V _{DD}	V	3, 4

Note:

- For input only pins except RESET#. V_{ref} = V_{refCA}(DC).
- See "Overshoot and Undershoot Specifications" in the device datasheet.
- The ac peak noise on V_{ref} may not allow V_{ref} to deviate from V_{refDQ}(DC) by more than +/-1% V_{DD} (for reference: approx. +/- 15 mV).
- For reference: approx. V_{DD}/2 +/- 15 mV.

Single-Ended AC and DC Input Levels for DQ and DM

Symbol	Parameter	DDR3-1066 (-BE)		DDR3-1333 (-CG)		Units	Note
		Min.	Max.	Min.	Max.		
V _{IH.DQ} (DC)	DC Input Logic High	V _{ref} + 0.100	V _{DD}	V _{ref} + 0.100	V _{DD}	V	1
V _{IL.DQ} (DC)	DC Input Logic Low	V _{SS}	V _{ref} - 0.100	V _{SS}	V _{ref} - 0.100	V	1
V _{IH.DQ} (AC)	AC Input Logic High	V _{ref} + 0.175	Note 2	V _{ref} + 0.15	Note 2	V	1, 2, 5
V _{IL.DQ} (AC)	AC Input Logic Low	Note 2	V _{ref} - 0.175	Note 2	V _{ref} - 0.15	V	1, 2, 5
V _{RefDQ} (DC)	Reference Voltage for DQ, DM Inputs	0.49 x V _{DD}	0.51 x V _{DD}	0.49 x V _{DD}	0.51 x V _{DD}	V	3, 4

Note:

- For input only pins except RESET#. V_{ref} = V_{refDQ} (DC).
- See "Overshoot and Undershoot Specifications" in the device datasheet.
- The ac peak noise on V_{ref} may not allow V_{ref} to deviate from V_{refDQ}(DC) by more than +/-1% V_{DD} (for reference: approx. +/- 15 mV).
- For reference: approx. V_{DD}/2 +/- 15 mV.
- Single-ended swing requirement for DQS, DQS# is 350 mV (peak to peak). Differential swing requirement for DQS - DQS# is 700 mV (peak to peak).

Operating, Standby, and Refresh Currents

$T_{CASE} = 0^{\circ}C \sim 85^{\circ}C$; $V_{DDQ} = V_{DD} = 1.5V \pm 0.075V$ (2GB, 2 Ranks, base on 128Mx8 DDR3 SDRAMs)

Symbol	Parameter/Condition	DDR3-1066	DDR3-1333	Unit
I _{DD0}	Operating Current: one bank activate/Precharge	1364	1496	mA
I _{DD1}	Operating Current: one bank activate/Read/Precharge	1540	1672	mA
I _{DD2P(0)}	Precharge Power-Down Current Fast Exit-MR0 bit A12=0	211	211	mA
I _{DD2P(1)}	Precharge Power Down Current Slow Exit-MR0 bit A12=1	440	528	mA
I _{DD2N}	Precharge Standby Current	968	1056	mA
I _{DD2Q}	Precharge Quiet Standby current	880	968	mA
I _{DD3P}	Active Power-Down Current Always Fast Exit	528	616	mA
I _{DD3N}	Active Standby Current	968	1056	mA
I _{DD4W}	Operating Current: Burst Write	1892	2288	mA
I _{DD4R}	Operating Current: Burst Read	1892	2200	mA
I _{DD5B}	Burst Refresh Current	2420	2640	mA
I _{DD6}	Self-Refresh Current Normal Temperature Range (0-85C)	176	176	mA
I _{DD7}	All Bank Interleave Read Current	3916	4840	mA

Speed Bins

Speed Bin			DDR3-1066(-BE)		DDR3-1333 (-CG)		Unit
CL - nRCD - nRP			7-7-7		9-9-9		
Parameter		Symbol	Min	Max	Min	Max	
Internal read command to first data		tAA	13.125	20	13.125	20	ns
ACT to internal read or write delay time		tRCD	13.125	--	13.125	--	ns
PRE command period		tRP	13.125	--	13.125	--	ns
ACT to ACT or REF command period		tRC	50.625	--	49.125	--	ns
ACT to PRE command period		tRAS	37.5	9*tREFI	36	9*tREFI	ns
CL = 6	CWL=5	tCK(AVG)	2.5	3.3	2.5	3.3	ns
	CWL=6	tCK(AVG)	Reserved		Reserved		ns
	CWL=7, 8	tCK(AVG)	Reserved		Reserved		ns
CL = 7	CWL=5	tCK(AVG)	Reserved		Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	1.875	<2.5	ns
	CWL=7	tCK(AVG)	Reserved		Reserved		ns
	CWL=8	tCK(AVG)	Reserved		Reserved		ns
CL = 8	CWL=5	tCK(AVG)	Reserved		Reserved		ns
	CWL=6	tCK(AVG)	1.875	<2.5	1.875	<2.5	ns
	CWL=7	tCK(AVG)	Reserved		Reserved		ns
	CWL=8	tCK(AVG)	Reserved		Reserved		ns
CL = 9	CWL=5, 6	tCK(AVG)	Reserved		Reserved		ns
	CWL=7	tCK(AVG)	Reserved		1.5	<1.875	ns
	CWL=8	tCK(AVG)	Reserved		Reserved		ns
Supported CL settings			6,7,8		6,7,8,9		nCK
Supported CWL Settings			6		6,7		nCK

AC Timing Specifications for DDR3 SDRAM Devices Used on Module

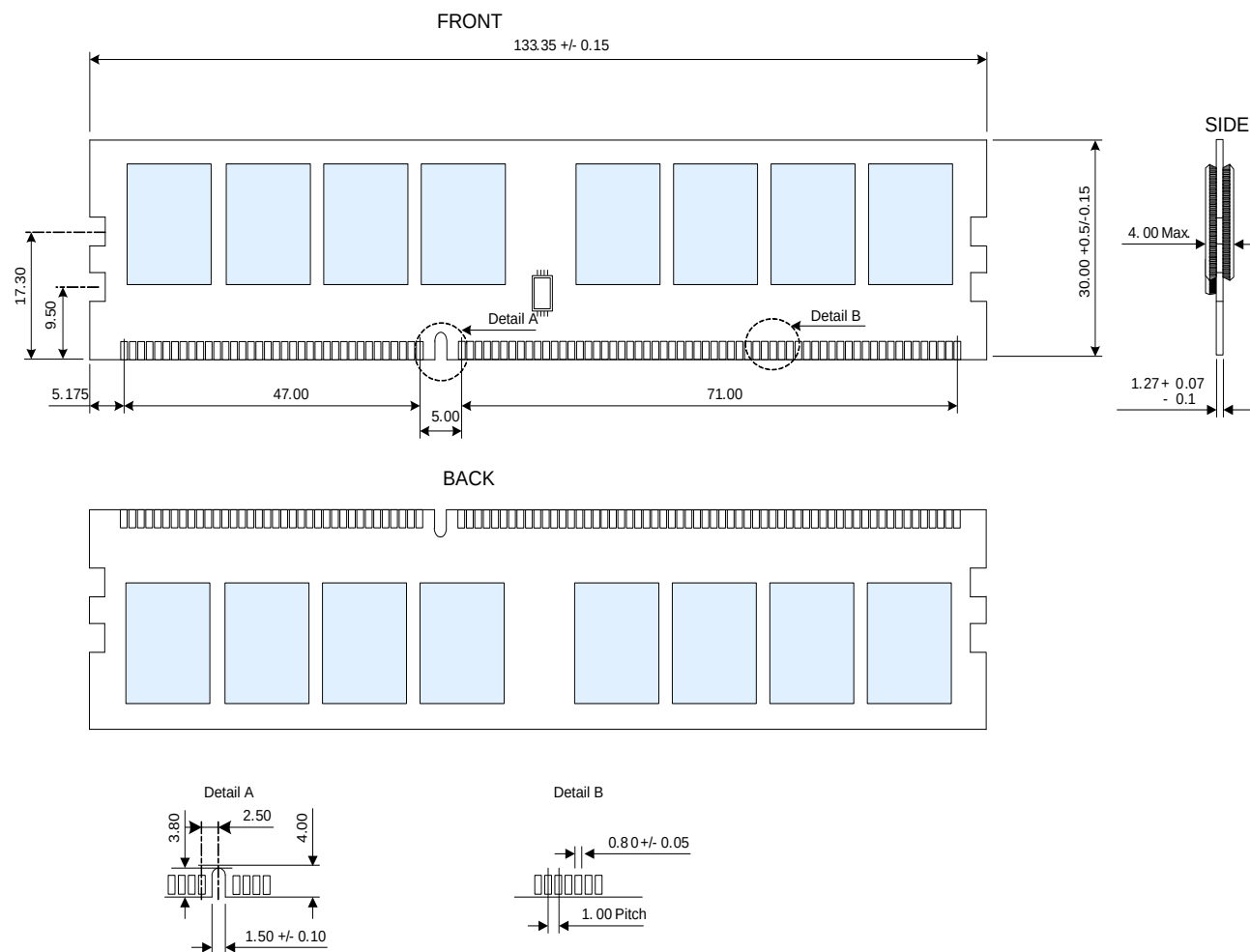
		DDR3-1066		DDR3-1333		
Parameter	Symbol	Min	Max	Min	Max	Units
Clock Timing						
Minimum Clock Cycle time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	ns
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min +tJIT(per)min	tCK(avg)max +tJIT(per)max	tCK(avg)min +tJIT(per)min	tCK(avg)max +tJIT(per)max	ps
Absolute clock high pulse width	tCH(abs)	0.43	-	0.43	-	ps
Absolute clock low pulse width	tCL(abs)	0.43	-	0.43	-	ps
Clock Period Jitter	tJIT(per)	-90	90	-80	80	ps
Clock Period Jitter during DLL locking period	tJIT(per,lck)	-80	80	-70	70	ps
Cycle to Cycle Period Jitter	tJIT(cc)	180		160		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc,lck)	160		140		ps
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	ps
Cumulative error across 2 cycles	tERR(2per)	-132	132	-118	118	ps
Cumulative error across 3 cycles	tERR(3per)	-157	157	-140	140	ps
Cumulative error across 4 cycles	tERR(4per)	-175	175	-155	155	ps
Cumulative error across 5 cycles	tERR(5per)	-188	188	-168	168	ps
Cumulative error across 6 cycles	tERR(6per)	-200	200	-177	177	ps
Cumulative error across 7 cycles	tERR(7per)	-209	209	-186	186	ps
Cumulative error across 8 cycles	tERR(8per)	-217	217	-193	193	ps
Cumulative error across 9 cycles	tERR(9per)	-224	224	-200	200	ps
Cumulative error across 10 cycles	tERR(10per)	-231	231	-205	205	ps
Cumulative error across n=11~50 cycles	tERR(nper)	tERR(npr)min =(1+0.68ln(n))*tJIT(per)min	tERR(npr)max =(1+0.68ln(n))*tJIT(per)max	tERR(npr)min =(1+0.68ln(n))*tJIT(per)min	tERR(npr)max =(1+0.68ln(n))*tJIT(per)max	ps
Data Timing						
DQS, $\overline{DQS}$ to DQ skew, per group, per access	tDQSQ	-	150	-	125	ps
DQ output hold time from DQS, $\overline{DQS}$	tQH	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, $\overline{CK}$	tLZ(DQ)	-600	300	-500	250	ps
DQ high-impedance time from CK, $\overline{CK}$	tHZ(DQ)	-	300	-	250	ps
Data setup time to DQS, $\overline{DQS}$ reference to Vih(ac) / Vil(ac) levels	tDS(base) AC175	25	-	-	-	ps
Data hold time to DQS, $\overline{DQS}$ reference to Vih(ac) / Vil(ac) levels	tDS(base) AC150	75	-	30	-	ps
Data hold time from DQS, $\overline{DQS}$ referenced to Vih(dc) / Vil(dc) levels	tDH(base) DC100	100	-	65	-	ps
DQ and DM Input pulse width for each input	tDIPW	490	-	400	-	ps
Data Strobe Timing						
DQS, $\overline{DQS}$ differential READ Preamble	tRPRE	0.9	-	0.9	-	tCK(avg)
DQS, $\overline{DQS}$ differential READ Postamble	tRPST	0.3	-	0.3	-	tCK(avg)
DQS, $\overline{DQS}$ differential output high time	tQSH	0.38	-	0.40	-	tCK(avg)
DQS, $\overline{DQS}$ differential output low time	tQSL	0.38	-	0.40	-	tCK(avg)
DQS, $\overline{DQS}$ differential WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK(avg)
DQS, $\overline{DQS}$ differential WRITE Postamble	tWPST	0.3	-	0.3	-	tCK(avg)
DQS, $\overline{DQS}$ rising dege output access time from rising CK, $\overline{CK}$	tDQSCK	-300	300	-255	255	ps
DQS, $\overline{DQS}$ low-impedance time (Reference from RL-1)	tLZ(DQS)	-600	300	-500	250	ps
DQS, $\overline{DQS}$ high-impedance time (Reference from RL + BL/2)	tHZ(DQS)	-	300	-	250	ps
DQS, $\overline{DQS}$ differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	tCK(avg)
DQS, $\overline{DQS}$ differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	tCK(avg)

Parameter	DDR3-1066			DDR3-1333		
	Symbol	Min	Max	Min	Max	Units
Data Strobe Timing						
DQS, $\overline{\text{DQS}}$ rising edge to CK, $\overline{\text{CK}}$ rising edge	tDQSS	-0.25	0.25	-0.25	0.25	tCK(avg)
DQS, $\overline{\text{DQS}}$ falling edge setup time to CK, $\overline{\text{CK}}$ rising edge	tDSS	0.2	-	0.2	-	tCK(avg)
DQS, $\overline{\text{DQS}}$ falling edge hold time to CK, $\overline{\text{CK}}$ rising edge	tDSH	0.2	-	0.2	-	tCK(avg)
Command and Address Timing						
DLL locking time	tDLLK	512	-	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)	-	max(4nCK, 7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	nCK
Mode Register Set command update delay	tMOD	max(12nCK, 15ns)	-	max(12nCK, 15ns)	-	
$\overline{\text{CAS}}$ to $\overline{\text{CAS}}$ command delay	tCCD	4	-	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP/tCK(avg))				nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max(4nCK, 7.5ns)	-	max(4nCK, 6ns)	-	
Four activate window for 1KB page size	tFAW	37.5	-	30	-	ns
Command and Address setup time to CK, $\overline{\text{CK}}$ referenced to Vih(ac) / Vil(ac) levels	tIS(base)	125	-	65	-	ps
Command and Address hold time to CK, $\overline{\text{CK}}$ referenced to Vih(ac) / Vil(ac) levels	tIH(base)	200	-	140	-	ps
Calibrating Timing						
Power-up and RESET calibration time	tZQinit	512	-	512	-	nCK
Normal operation Full calibration time	tZQoper	256	-	256	-	nCK
Normal operation Short calibration time	tZQCS	64	-	64	-	nCK
Reset Timing						
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	
Self Refresh Timings						
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min) + 1nCK	-	tCKE(min) + 1nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
Valid Clock Requirement after Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK, 10ns)	-	max(5nCK, 10ns)	-	
Power Down Timings						
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK, 7.5ns)	-	max(3nCK, 6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK, 24ns)	-	max(10nCK, 24ns)	-	
CKE minimum pulse width	tCKE	max(3nCK, 5.625ns)	-	max(3nCK, 5.625ns)	-	
Command pass disable delay	tCPDED	1	-	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(a vg))	-	WL+4+(tWR/tCK(a vg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+(tWR/tCK(a vg))	-	WL+2+(tWR/tCK(a vg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL+2+WR+1	-	WL+2+WR+1	-	nCK
Timing of REF command to Power down entry	tREFPDEN	1	-	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	

		DDR3-1066		DDR3-1333		
Parameter	Symbol	Min	Max	Min	Max	Units
ODT Timings						
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK
Asynchronous RTT turn-on delay (Power - Down with DLL frozen)	tAONPD	2	8.5	2	8.5	ns
Asynchronous RTT turn-off delay (Power – Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	ns
RTT turn-on	tAON	-300	300	-250	250	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timings						
First DQS/DQS rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	nCK
DQS/DQS delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	nCK
Write leveling setup time from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	tWLS	245	-	195	-	ps
Write leveling setup hold from rising CK, $\overline{CK}$ crossing to rising DQS, $\overline{DQS}$ crossing	tWLH	245	-	195	-	ps
Write leveling output delay	tWLO	0	9	0	9	ns
Write leveling output error	tWLOE	0	2	0	2	ns

Package Dimensions

(2GB, 2 Ranks, 128Mx8 DDR3 SDRAMs, M2Y2G64CB8HC5N-BE/CG)



Units: Millimeters

Note: Device position is only for reference.

Revision Log

Rev	Date	Modification
0.1	11/2009	Preliminary Edition
1.0	01/2010	Official Release
1.1	01/2010	Revision Updated